Using Multilayer Baluns to Improve ADC Performance

September, 2009

Introduction

This application note explains the use of Anaren's multilayer balun (BD0205F5050AHF) in conjunction with Analog Devices AD9640 integrated dual 14-bit, 80/105/125/150 MSPS analog to digital converter. The AD9640 ADC (Analog to Digital Converter) operates up to a 125 MSPS conversion rate and is optimized for use in diversity radio systems, smart antennas, multimode digital receivers, and software radio systems.

This application note will show that use of Anaren's BD0205F5050A00 balun will result in an improvement in SFDR (Spurious Free Dynamic Range) and gain flatness as compared to a traditional wirewound balun implementation. The BD0205F5050A00 is a new Anaren product that has been specifically designed for use in an ADC front end circuit.

In addition to improving ADC performance, it will be seen that Anaren's baluns offer superior part to part consistency through proven fabrication technology based on multilayer organic substrates. The same technology provides a balun with a sub 1mm height profile for height constrained applications. Anaren baluns, because of the achievable gain flatness, support wide bandwidths at higher frequency of operation for undersampling applications. This differentiation allows operation and performance repeatability not available in a wire-wound equivalent. A reduced overall component count also comes through a single Anaren balun replacing multiple wire-wounds parts while maintaining performance.

The AD9640 is an "unbuffered" ADC as opposed to "buffered" designs such as the AD9445 which results in greater challenges in matching the ADC to the balun / transformer. Issues such as "charge kickback" also present design challenges that need to be addressed by the ADC front end designer. Whereas the buffered ADC's are relatively easy to use, they do consume more power than the unbuffered ADC's and the specific application needs will dictate the ADC selection. However it has been shown in a previous Anaren application note [7] that the Anaren baluns provide improved performance for buffered ADC applications as well.

As a consequence of this, this application note shows how the matching network in conjunction with the balun can be used to optimize performance over various frequency bands for an unbuffered ADC, in this case the AD9640. Examples of matching networks are given.

In summary, it will be shown that use of Anaren's multi-layer components will offer the following benefits to the ADC front end designer:

- Improved high frequency amplitude and phase balance resulting in better SFDR
- Improved gain flatness thus reducing input drive requirements
- Smaller footprint and height than traditional wirewounds
- Inherently suited to SMT pick and place operations
- Highly repeatable manufacturing process resulting in little part to part variation
- Ferrite free design thus eliminating the possibility intermodulation and other non-linear effects
- Reduction in components used for frontend design

Role of Baluns in ADC Design

Baluns (or transformers) are passive devices that a) provide an impedance transformation and b) convert a single ended signal into a differential one. Baluns are used in analog to digital conversion circuits to couple signals appropriately to the converter's differential analog inputs. In this discussion, the terms balun and transformer will be used interchangeably.

Single ended signals travel on an individual trace with a certain characteristic impedance, usually 50Ω. However, a two conductor system can carry "differential signals". In this configuration, the currents and voltages on the differential lines are 180° out of phase and are of equal magnitude.

Conversely, common mode signals have voltages and currents on the differential lines which are in phase. The balun may be thought of a common mode filter which rejects common mode signals on the differential lines but allows differential signals to pass.

As stated in the Analog Devices datasheet for the AD9640 [8], since the analog inputs to the ADC are differential, significant performance improvements result from the differential analog stages having a high rejection of even-order harmonics. Differential inputs have high common mode rejection of stray signal, such as ground and power noise.

At higher frequencies, the electrical performance of a balun is more conveniently characterized by microwave performance parameters such as return loss, insertion loss, phase and amplitude balance, and common mode rejection ratio or common mode rejection/attenuation. Insertion loss is a description of signal attenuation through the balun and as such can be used to define the bandwidth of the component. Unbalanced return loss defines how much RF power is reflected from signals incident on the unbalanced, single ended port. Conversely, balanced return loss defines how much RF power is reflected from the balanced, differential port. Return loss describes how well the port impedances of the balun are matched to other components.

Finally, amplitude and phase balance are indicators of how well the balun transforms a signal from single ended to differential. As mentioned above ideally, the signals on the two differential lines should be equal and opposite. To this end, a simple ratio of the amplitudes of the signals will provide a measure of the amplitude balance with 1 or (0 dB if a logarithmic scale is being used) being the ideal value. Similarly, ideally the phase difference between the differential pairs should be 180°.

Effect of Balun Amplitude & Phase Balance on ADC Performance

The performance of ADCs is heavily influenced by amplitude and phase imbalances arising from the balun, especially in high frequency applications. Specifically, non-linearities in the ADC will cause even harmonics to be generated if the balun has amplitude or phase imbalance. The presence of harmonics will adversely affect ADC performance parameters such as SFDR, SNR, THD, and SINAD (See Section "ADC Performance Parameter Definitions" for definitions of these parameters).

Reeder and Ramachandran [1] investigate the effect of non-ideal amplitude and phase balance on ADC performance by modeling the ADC as a symmetrical third order transfer function and the differential output signals as sinusoids. Following the nomenclature of [1], the ADC transfer function and differential sinusoids are defined as:

$$h(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)$$

$$x_1(t) = k_1 \sin(\omega t)$$

$$x_2(t) = k_2 \sin(\omega t - 180° + \phi)$$

where h(t) is the ADC transfer function, $x_1(t)$ and $x_2(t)$ are the differential sinusoids. In the ideal differential case, $k_1 = k_2$ and $\varphi = 0$. The non-linear $x^2(t)$ and $x^3(t)$ terms give rise to harmonics.

The following conclusions are made in their paper:

1. In the ideal case (i.e. perfect phase and amplitude balance) , even harmonics cancel out, while the odd ones do not, i.e. when $k_1 = k_2$ & $\varphi = 0°$
2. In the case of a magnitude imbalance and no phase imbalance, the second harmonic is proportional to k_1^2 and k_2^2, specifically

   $$2f_0 \propto k_1^2 - k_2^2$$

   where k_1 and k_2 are the amplitudes of the differential pair signal.
3. In the case of phase imbalance and no magnitude imbalance, the second harmonic is in proportion to k_1^2, i.e.

   $$2f_0 \propto k_1^2$$

where f_0 is the fundamental frequency.

Note from the above that since $k_1^2 > k_1^2 - k_2^2$, a phase imbalance condition will yield a larger second harmonic than an amplitude imbalance condition. Emphasis then should be placed on minimizing phase balance errors.

The generation of harmonics will have a direct and adverse effect on SFDR and SNR. SFDR and SNR are defined in the Section "ADC Performance Parameter Definitions". Generally, the higher the level of spurious harmonics, the greater the degradation in SNR and SFDR which in turn affect ADC performance.

It is clear that a significant performance enhancement of ADCs can be obtained through the choice of a balun or transformer with the best possible amplitude and phase characteristics over the bandwidth required.

The next section describes advantages of multilayer stripline microwave structures over wirewound technology especially at higher frequencies.

Wire Wound Balun vs. Anaren Balun Performance Comparison

Wire Wound Balun

Until recently, wire wound transformers have been typically the solution of choice in ADC converter front end circuit design to convert single ended signals to differential signals. The transformation ratios are typically 1:1, although 1:4 transformations are also popular and are used to provide a voltage step-up to minimize the input drive power required from the preceeding stage. Most wire wound baluns deliver good performance at lower frequencies (i.e. < 200 MHz) where they exhibit good balanced phase and amplitude performance with good insertion and return loss.

However, wire wound baluns suffer from some drawbacks, the most serious of which is the deterioration of performance at higher frequencies. Wire wound baluns are essentially lumped element components which work well at lower frequencies, but whose performance deteriorates as the effects of parasitics in combination with PCB parasitics become more pronounced at higher frequencies and ferrite losses increase. Lumped element components are not suited for use as the wavelength of operation becomes comparable to the physical dimensions of the component, i.e. when one operates in the microwave region.

Other drawbacks include the fact that often the dome shaped ferrite core is not well suited to for high volume pick-and-place manufacturing equipment[6]. Anaren's multilayer stripline structure are inherently amenable to being used as surface mount devices and because current multilayer softboard manufacturing methods are used, these devices can be made in an extremely repeatable manner thus ensuring part-to-part consistency.

Finally, because wirewound baluns have a non-linear ferrite core, they are vulnerable to performance variations over temperature and intermodulation effects because of the non-linear nature of ferrites.

Anaren Balun – BD0205F5050A00 (Merrill type)

The Anaren BD0205F5050A00 is a new product specifically designed for use in ADC front end circuits. These baluns are coupled, microwave stripline structures and as such are inherently suited for operation across wider bands.

They are coupled stripline designs which use softboard (PTFE / Teflon) type material as the dielectric medium. The dielectric chosen for the design has a low loss tangent thus ensuring that insertion loss is kept to a minimum at higher frequencies. In addition, the use of proprietary design techniques allows significant amount of circuitry to be packed into a small package.

The Merrill structure was chosen in order to maximize bandwidth at the 1:1 impedance ratio, while maintaining a very good balanced performance. This balun structure is discussed below.

Merrill Balun Structure

There are many different topologies that can be used to implement baluns in a surface mount format such as the Marchand, Guanella, Ruthroff and finally the inverted or Merrill structures which is the topology for the BD0205F5050A00.

The Merrill balun geometry used in BD0205F5050A00 is a structure that converts single-ended to

differential signal using two backward wave couplers [5]. Shown below are a pair of couplers with characteristic impedance Z_0. Initially, this may be considered to be an 8 port device.

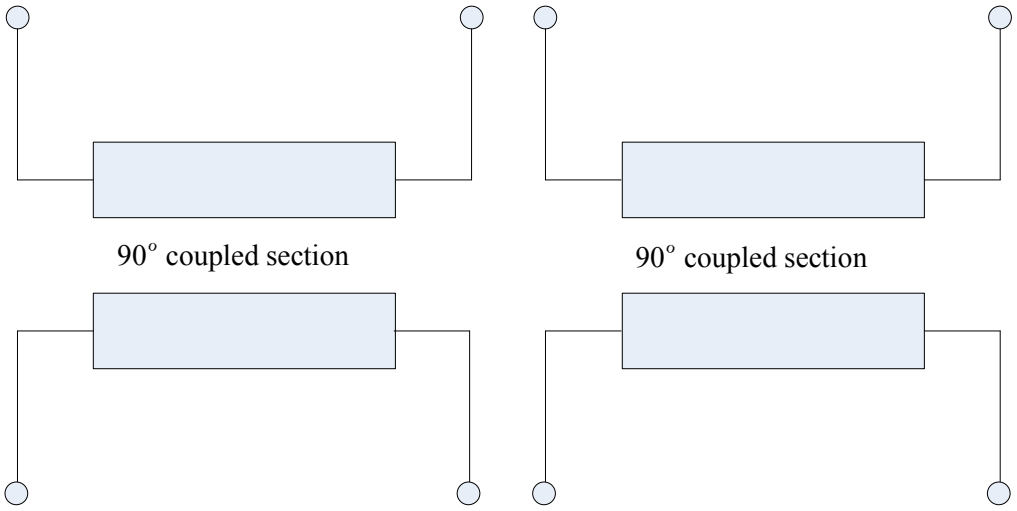


Figure 1 Two backward wave couplers

By shorting 3 of the ports and connecting the 2 couplers as shown in Figure 2, we are left with a 3 port device which will have the balun function that is desired.

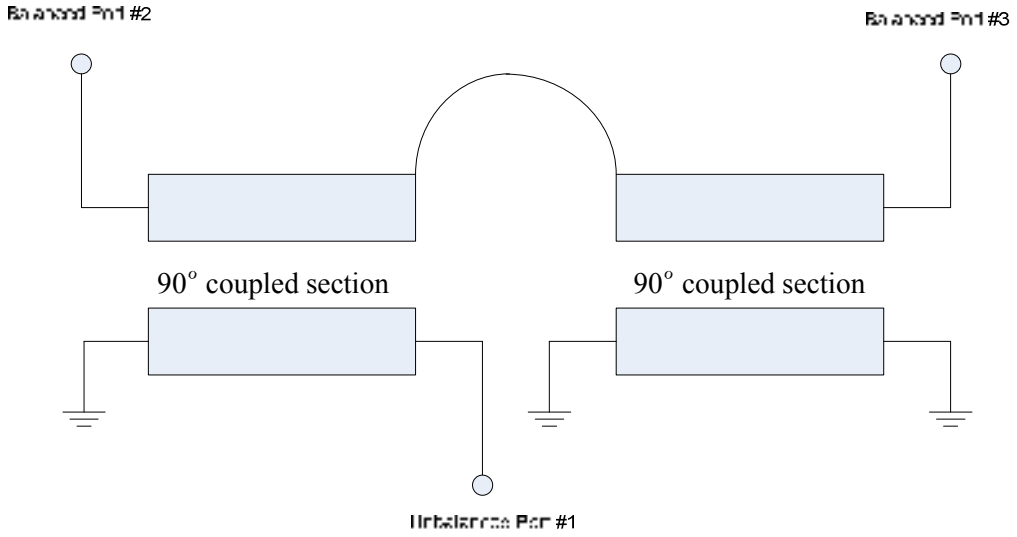


Figure 2 Interconnection Scheme

As noted before, the structures above are stripline couplers. The internal layout is deliberately made as symmetrical as possible in order to obtain excellent amplitude and phase balance. By altering coupling ratios, line lengths, line widths and spacings, the couplers can be optimized for various impedances and frequency bands.

In the ideal lossless case, it can be shown that the S-parameter matrix of the above 3 port is given by [5]:

$$S = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21}^t & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} = \begin{bmatrix} 0 & \frac{j}{\sqrt{2}} & -\frac{j}{\sqrt{2}} \\ \frac{j}{\sqrt{2}} & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{j}{\sqrt{2}} & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix}$$

The following equalities can be shown to hold and are then valid at all frequencies:

$$S_{22} = S_{33} = -\frac{1}{2} \qquad (1)$$

$$S_{23}^t = S_{32} \qquad (2)$$

$$S_{21} = -S_{31} \qquad (3)$$

$$\left| S_{22} + S_{32} \right| = 1 \qquad (4)$$

Equation (1) is the well known result that when viewed as single ended terminals, the differential ports #2 and #3 have an inherent return loss of – 6 dB which is a well known result for baluns. Equation (2) is simply an expression of the symmetry of the structure while equation (3) states that the signals on Ports #2 and #3 are equal in magnitude and 180° out of phase which is the standard requirement for a balun.

It should be noted that the above equations are also valid when the ports are not perfectly matched to external loads. In fact, a significant advantage of the Merrill balun structure is that it is relatively insensitive to changes in differential impedance as will be shown in the following section.

Merrill Balun Insensitivity to Changes in Differential Impedance

Insensitivity to variations in differential impedances is a major advantage of a Merrill implementation over wirewound transformers because the impedances presented to the balun/transformer by an "unbuffered" ADC change as the ADC switches between sample, and hold. Any sensitivity on part of the balun/transformer to ADC impedances will reveal itself in degradation of converter performance.

As an example of this, shown below in Figure 3 is a Monte Carlo analysis of the effect of varying the differential impedance for BD0205F5050A00 and a representative wirewound balun.

To obtain these results, S-parameter measurements were obtained for both the BD0205F5050A0 balun and the wirewound balun using a network analyzer. These measured S-parameters were then used in a circuit simulator (Genesys) which was then used to generate a random set of differential impedances with which to terminate the balun.

Since the BD0205F5050A00 is designed for a 50Ω differential impedance, a ±15% variation centered on 50Ω was chosen. A "uniform" distribution of 200 random values was generated and the 200 performance curves plotted as shown in Figure 3.

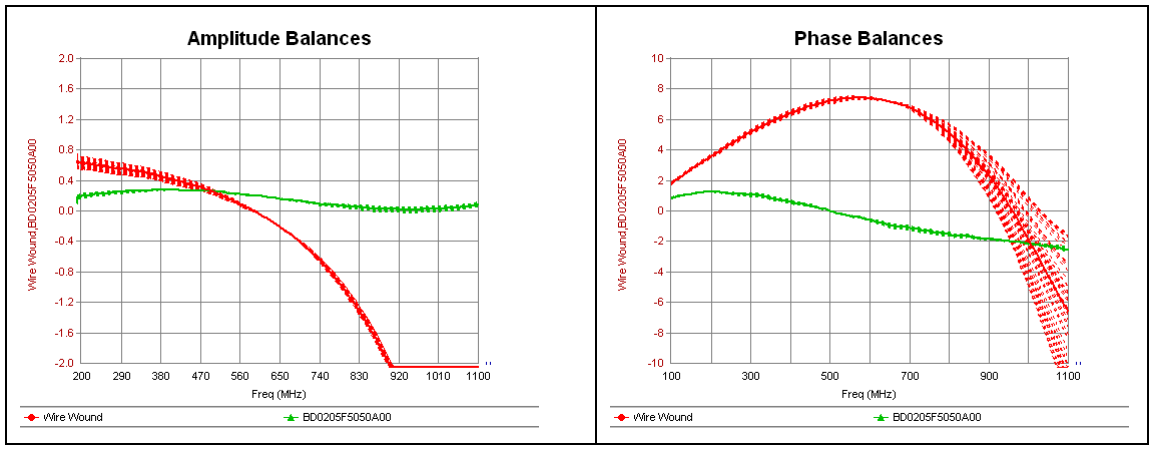


Figure 3 Monte Carlo Analysis of the Amplitude Balance and Phase Balance of a Wirewound transformer vs. BD0205F5050A00

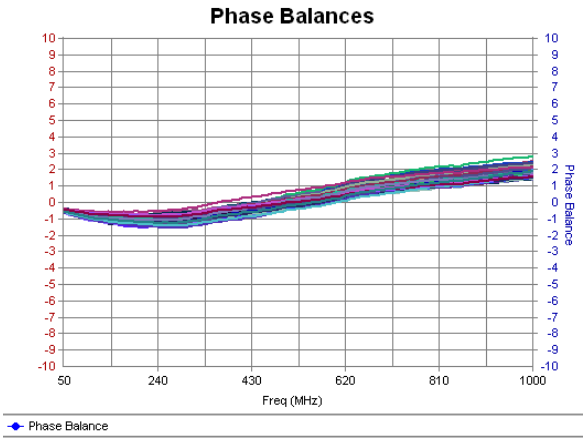
It can be seen that the variation of amplitude balance and phase balance as a function of differential impedance is larger for the wire wound balun than for the BD0205F5050A00. Note especially the sensitivity of the wirewound phase balance at the higher frequencies where we see an 8 degree variation at 1.1 GHz. As pointed out in a previous section, this can have significant effect on ADC performance.

Repeatability

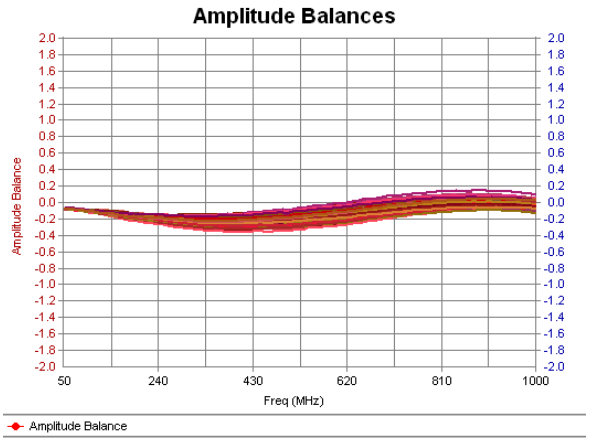
In addition to the above advantages, multilayer structures such as these have highly repeatable performance. Current lithography techniques allow for very compact, very repeatable structures to be manufactured in a very small package thus resulting in RF performances that are virtually identical from part to part. In turn this will result in ADC performance that is consistent from board to board.

Furthermore, because of the accuracy of the lithography and etching of the striplines, a great degree of symmetry can be achieved in the pair of couplers shown in Figure 2. This symmetry leads to, in turn, a high degree of amplitude and phase balance. Finally, this leads to a better frontend design and ultimately better converter performance.

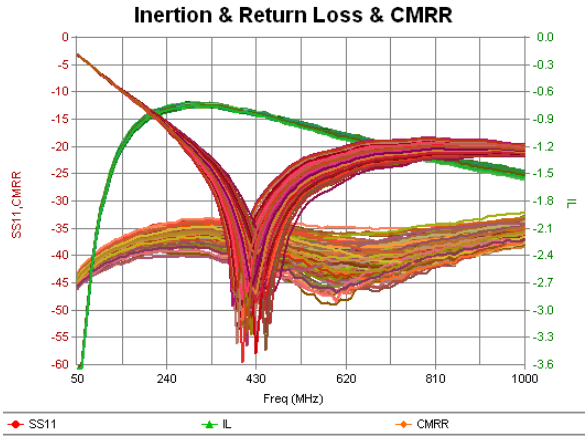
As an example of this repeatability, Figure 4 below shows a plot of the overlaid RF data for 180 parts of BD0205F5050A00.



Phase Balance 50 MHz – 1000 MHz 180 parts



Phase Balance 50 MHz – 1000 MHz 180 parts



Insertion, Return Loss & CMRR 50 MHz – 1000 MHz 180 parts

Figure 4 Plot of 180 BD0205F5050A00 showing repeatability of insertion loss, return loss and amplitude and phase balances.

It can be seen from the above plot that variation of insertion loss over the 180 parts is about ±0.05 dB, while amplitude balance is constant to within ±0.1 dB. Phase is constant to within ±1°.

Size & Volume Considerations

In addition to the above multilayer, stripline baluns offer a smaller footprint than wirewounds. For example, Anaren BD0205F5050A00 balun is in a 1608 package.

Table 1 compares the dimensions of the two different Anaren baluns with those of the wire wound baluns. Table 2 shows the percentage reductions in area required by using Anaren baluns

Table 1 Size Comparison Between Wire Wound Baluns and Anaren Baluns

	Length	Width	Height	PCB Area
BD0205F5050A00	0.157”	0.079”	0.029”	0.0124 sq. in.
MA/Com ETC1-1-13 Double Balun	2 X 0.150” = 0.300”	2 X 0.150” = 0.300”	0.105”	0.0900 sq. in
Mini-Circuits ADT-1-1	0.310”	0.220”	0.112”	0.0682 sq. in

Table 2 Space Savings Achieved by using Anaren Baluns

	MA/Com ETC1-1-13	Mini-Circuits ADT-1-1
BD0205F5050A00	Anaren 85% smaller	Anaren 82% smaller

Shown below Figure 5 is a pictorial comparison of the circuit board real estate requirements between the MA/Com ETC1-1-13, Mini-Circuits ADT-1-1, and BD0205F5050A00. It can be seen that the Anaren balun clearly requires less area than either wirewound balun.

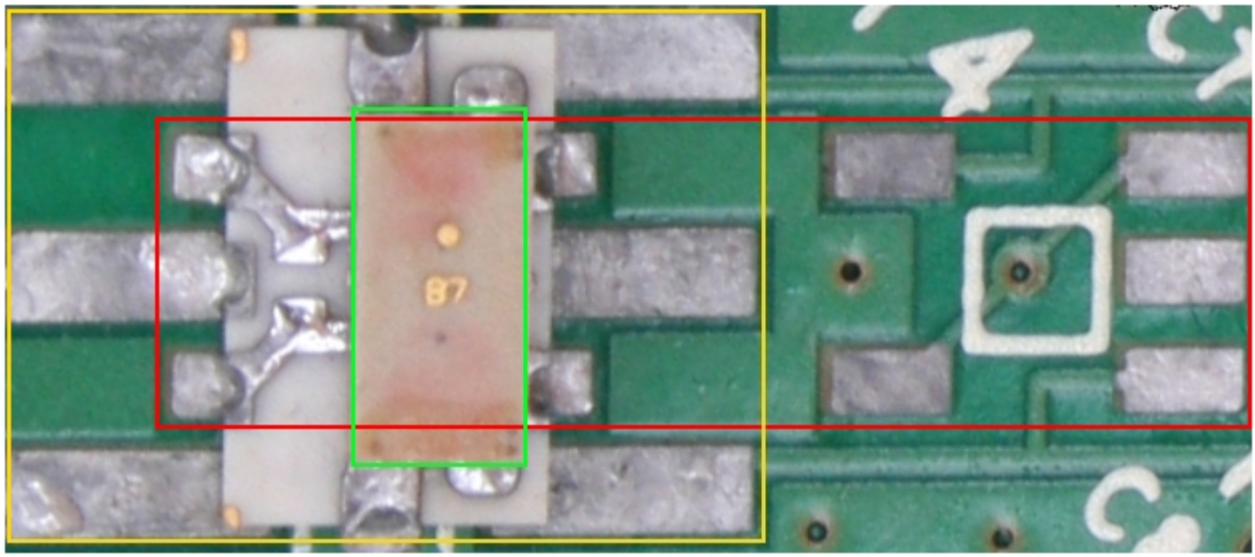


Figure 5 Comparison of Real Estate Requirements for MA/Com ETC1-1-13 (red), Mini-Circuits ADT1-1WT (yellow), and Anaren BD0205F5050A00 (green) balun

Matching Networks for BD0205F5050A00

This section discusses matching the BD0205F5050A00 balun to the AD9640 ADC converter using different matching networks optimized to various parameters of interest. Results demonstrating improved ADC performance over the baseline wirewound configuration are presented.

Reference Design Matching Network

The baseline balun for the AD9640 reference design is a dual MA/Com ETC1-1-13 wirewound transformer in a Guanella configuration with the matching network shown below:

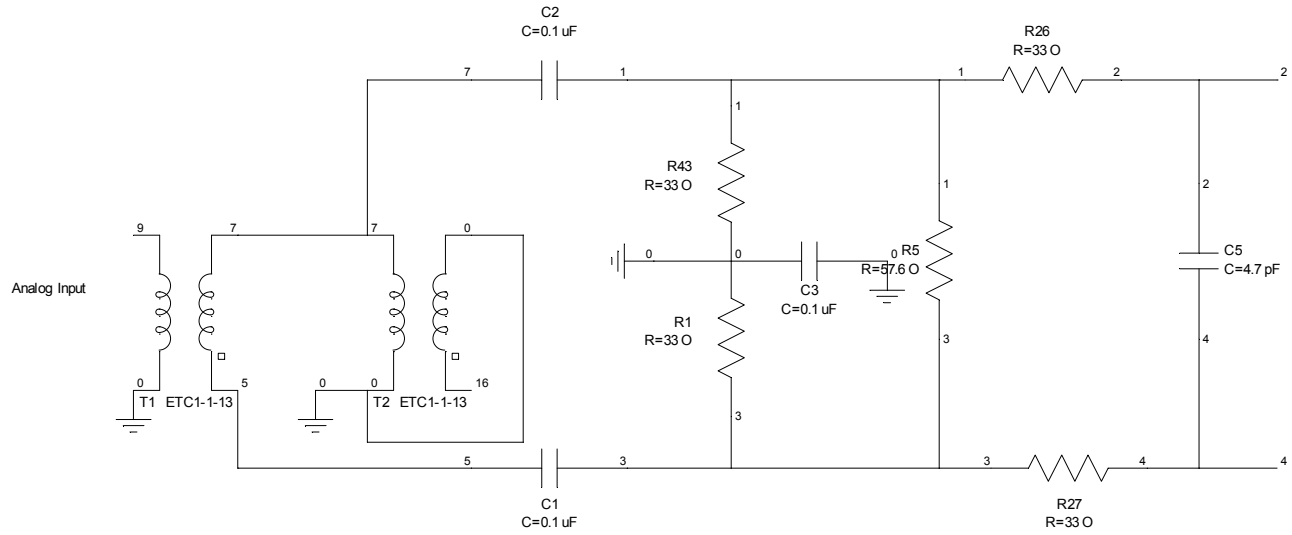


Figure 6 Reference Design Matching Network using ETC1-1-13 dual baluns

The capacitive / resistive matching network shown above in Figure 6 has a dual purpose. The first purpose is to match the transformer impedance to the input impedance of the AD9640 thus ensuring good RF performance at high frequencies. The second purpose is to filter out and attenuate the effects of "charge injection". As mentioned in the introduction, this charge kickback is due to the fact that the ADC is unbuffered and therefore the switching network inside the ADC sees the balun directly.

This filtering function is accomplished primarily by the resistor / capacitor network shown above which filters the "kickback". Minimizing this "kickback" will have the effect of improving SFDR and other performance parameters.

The BD0205F5050A00 is amenable to being both "tuned" for optimized performance a specific frequency band or being optimized for good performance over a wider band.

In order to demonstrate this flexibility, two different matching networks were designed for the BD0205F5050A00 to be used in conjunction with the AD9640:

1. narrowband or bandpass tuned design
2. wideband solution

These will now be described in greater detail in the section below.

Alternative Matching Networks

Narrowband Tuned

This solution was optimized for the 170 – 225 MHz band. The matching network for this solution is shown below:

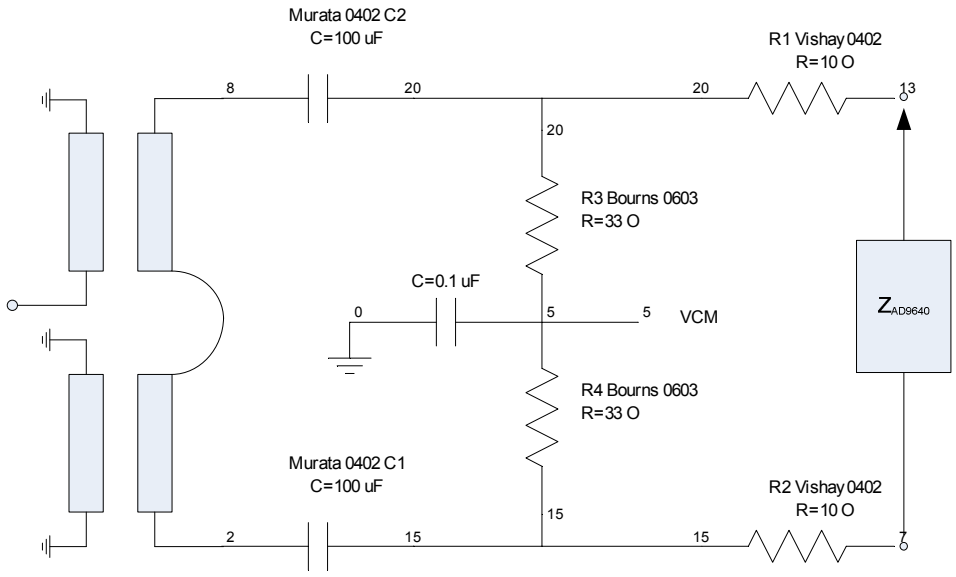


Figure 7 Narrow Band Tuned Solution using BD0205F5050A00

The schematic on the left represents the Merrill balun. On the right is the impedance of the AD9640 with the RLC network between being the actual matching network. The input impedance of the AD9640, Z_{AD9640}, was obtained by direct measurement using a "connecterized" daughterboard mounted on the AD9640 evaluation board.

Three conditions were used as optimization parameters for this case:

1. IL <-1.0 dB for 170 MHz < f < 225 MHz
2. IL >15 dB for f > 340 MHz
3. RL < -20 dB for 170 MHz < f < 225 MHz

where IL is the insertion loss, and RL is the return loss.

Optimization was performed using the circuit simulator, Genesys. The goal here was to minimize insertion loss in order to reduce analog drive levels.

Wideband Optimized

Shown below is the matching circuit for wideband operation of the BD0205F5050A00. Optimization parameters were set as follows:

- IL < -1.0 dB 50 MHz < f < 500 MHz
- RL < -20 dB 50 MHz < f < 500 MHz

The goal here was to maximize the insertion loss (gain flatness) over the entire useful bandwidth of the BD0205F5050A00.

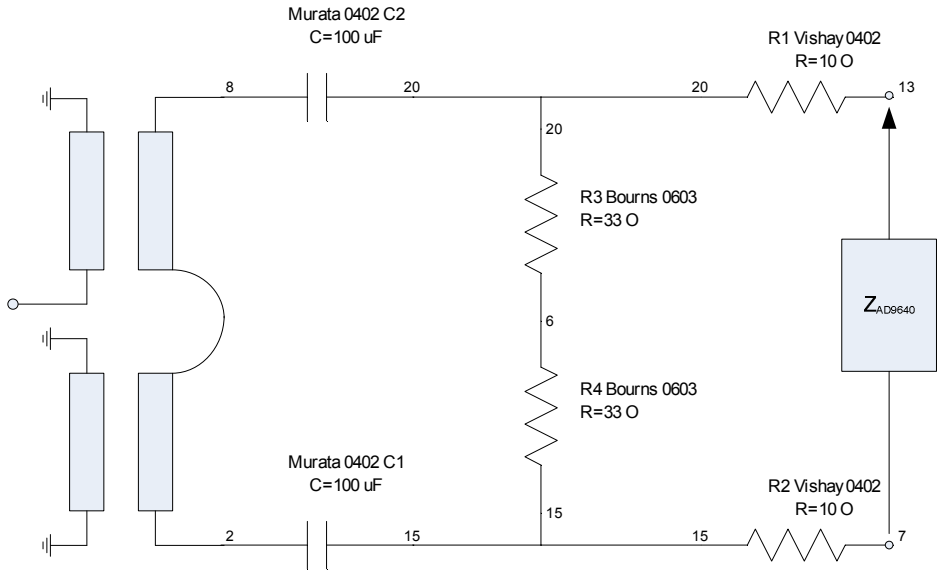


Figure 8 Wideband Optimized Matching Circuit using BD0205J5050A00

As before, Z_{AD9640} was obtained by measurement and Genesys was used to perform the optimization. Figure 8 shows the resulting circuit.

Measured Results

The sections below show the RF results and ADC performance parameters obtained for the two matching networks described in the previous section. In all cases, the BD0205F5050A00 balun was mounted on the AD9640 evaluation board with the appropriate matching network. RF results and ADC performance parameters were then obtained using the measurement techniques described in [3].

(Note: It should be emphasized that all comparisons shown in the following sections between Anaren's balun and wirewounds were done in identical conditions with identical equipment with the same AD9640 converter board to establish a baseline reference between the 2 components. Also shown in the Figures below are data points taken from the Analog Devices datasheet for the AD9640. This is shown only for reference. Because the datasheet data was obtained at a different times and possibly under different conditions, these points may not be directly comparable to the BD0205F5050A00 and wirewound results.)

SFDR Comparison

SFDR results obtained with BD0205F5050A00 with the two matching networks described above are compared to the wirewound balun baseline which in this case are 2 MA/Com ETC1-1-13 baluns connected as shown in Figure 6.

Narrow Band Tuned Design

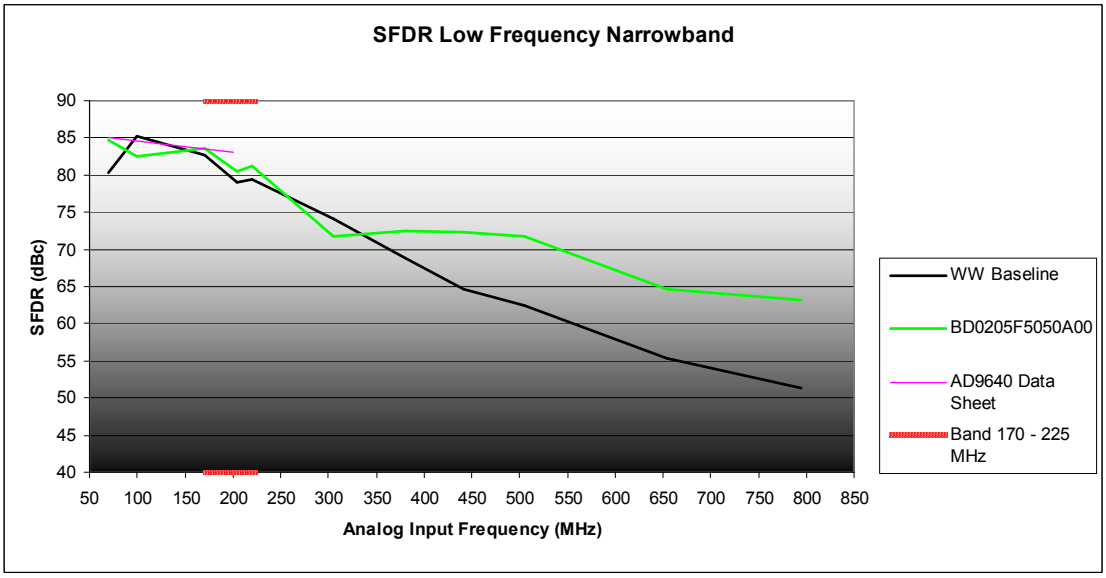


Figure 9 SFDR performance comparison: Wirewound baseline, BD0205F5050A00, and results reported on AD9640 datasheet

Shown in Figure 9 is the SFDR performance of the wirewound reference solution vs. the BD0205F5050A00 with the narrowband tuned network (the 170 – 225 MHz band is indicated by the red hatched line at the top and bottom of the plot). Shown also is the SFDR results reported in the AD9640 datasheet.

SFDR levels are at about 72 dBc at 450 MHz and at about the 64 dBc level at 650 MHz.

It can be seen that the BD0205F5050A00 does outperform the wirewound solution and is significantly better at the higher frequencies.

Wideband Optimized

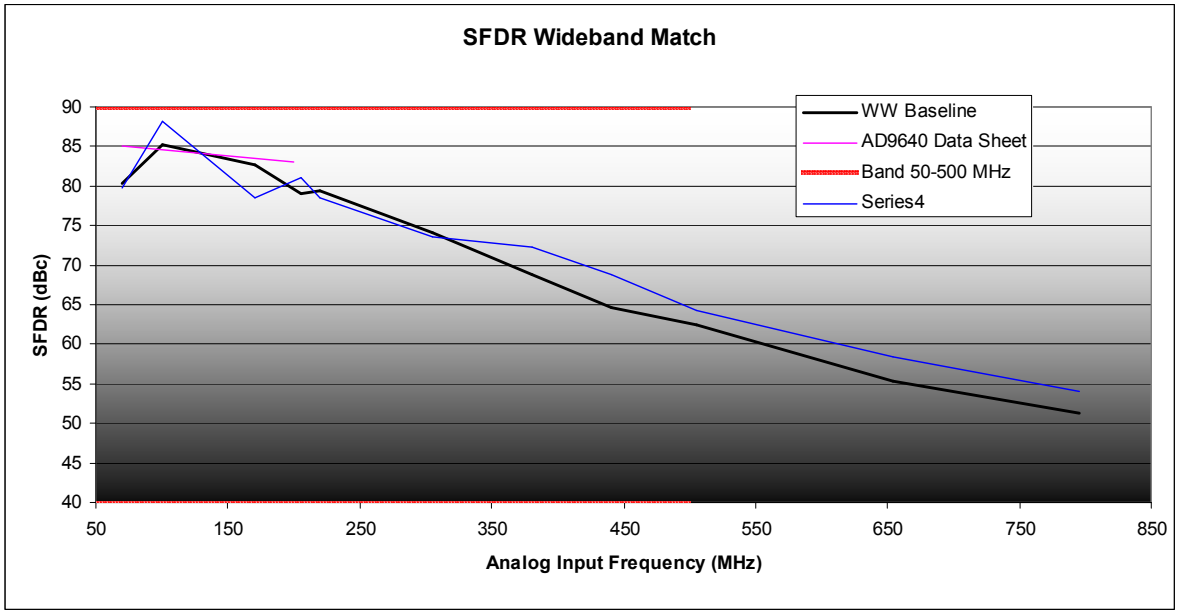


Figure 10 SFDR performance comparison for the optimized wideband match case. Shown are the wirewound baseline, BD0205F5050A00, and results reported on AD9640 datasheet

Show in Figure 10 is the SFDR performance of the wirewound reference solution vs. the BD0205F5050A00 with the wideband optimized network (the 50 – 500 MHz band is indicated by the red hatched line at the top and bottom of the plot). Shown also is the SFDR results reported in the AD9640 datasheet.

It can be seen that the SFDR is better than the baseline wirewound solution for frequencies above 300 MHz. It is interesting that the SFDR at higher frequencies is improved with the narrowband solution compared with the wideband solution. This may be a result of the narrow band solution attenuating more of the input signal at higher frequencies and therefore failing to reach full scale for the data converter. This lower signal level at the higher frequencies would therefore not drive nonlinearities in the ADC to same extent.

Gain Flatness

This test measures the loss through the matching network and the data converter for a particular balun or transformer. The measurement band is from 10 MHz to 1005 MHz.

The test is performed by setting the power level of the signal generator so that the peak signal value is -1 dB full scale, i.e. all other values in the band will be below -1 dB. A frequency of 1005MHz is used because it is well beyond the converter's bandwidth. A 100MHz reference setting was chosen at -1 dB full scale, i.e. all other values in the band will be referenced to that frequency (usually they will be equal or lower).

With the signal generator set at that value, a frequency sweep is performed over the 10 MHz to 1005 MHz bandwidth with signal level being recorded. Note that as expected the -1 dBFS (dB Full Scale) point is at the lowest frequency for the wirewound balun while for the Anaren baluns, the -1dBFS point is at about 200 MHz.

Narrowband Tuned Design

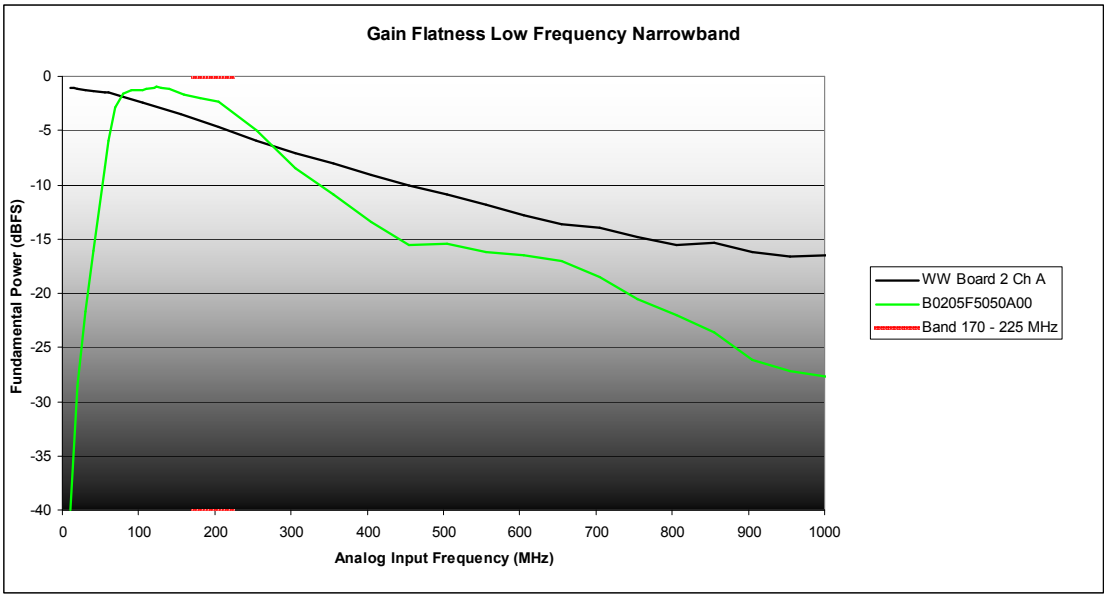


Figure 11 Gain Flatness: Low Frequency Narrowband solution, wirewound reference design vs. BD0205F5050A00

Shown above in Figure 11 is the gain flatness obtained when the BD0205F5050A00 balun is used in conjunction with the low frequency narrowband network as the front end to the ADC. It can be seen that the drive levels show a 2 dBi improvement above those of the wirewound solution . The 170 - 225 MHz optimization band is marked in the hatched redline at the top of the plot.

Wideband Optimized

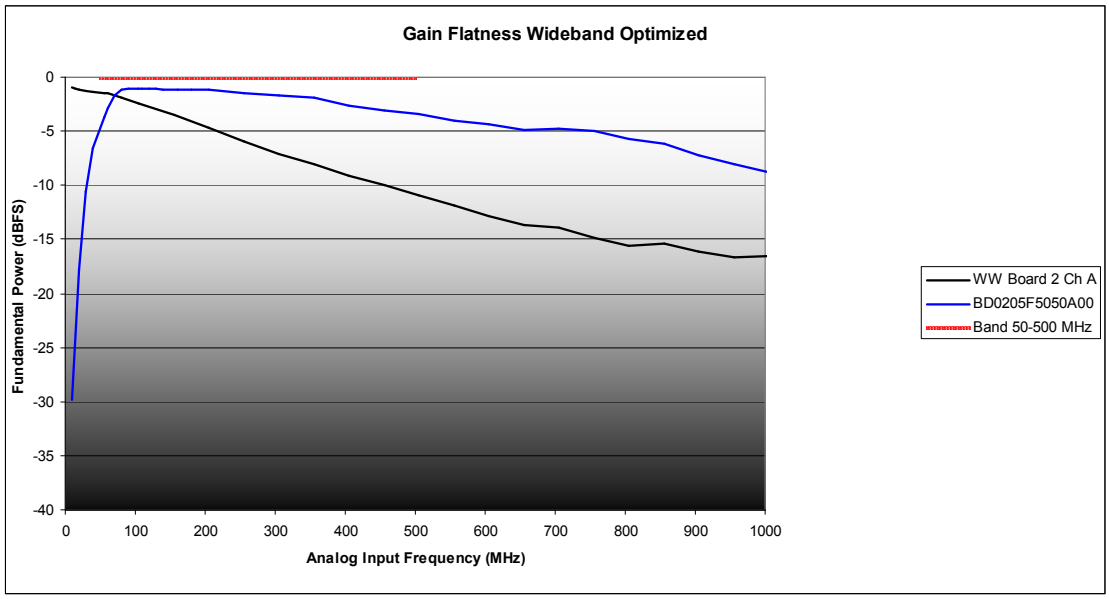


Figure 12 Gain Flatness: Wideband Optimized solution, wirewound reference design vs. BD0205F5050A00

Shown above in Figure 12 is the gain flatness obtained when the BD0205F5050A00 balun is used in conjunction with the wideband optimized network as the front-end to the ADC. It can be seen that the gain levels are significantly above those of the wirewound solution especially at the higher frequencies. The 50 MHz- 500 MHz optimization band is marked in the hatched redline at the top of the plot.

Signal to Noise Ratio

The following section describes signal to noise ratio obtained using the measurement techniques described in Reference [3].

As is seen below, the SNR measurements do not change much between the Anaren solutions and the wire wound balun solution. This is expected due to the passive nature of these solutions which should not add noise into the signal. One interesting effect of the input bandwidth to the matching network is that the Wideband Optimized solution has slightly worse SNR performance due less "filtering" from the matching network being convolved through the frequency range during the sampling process.

Figure 13 presents the results for the low frequency tuned solution while Figure 14 shows the wideband optimized solution.

Narrowband Tuned Design

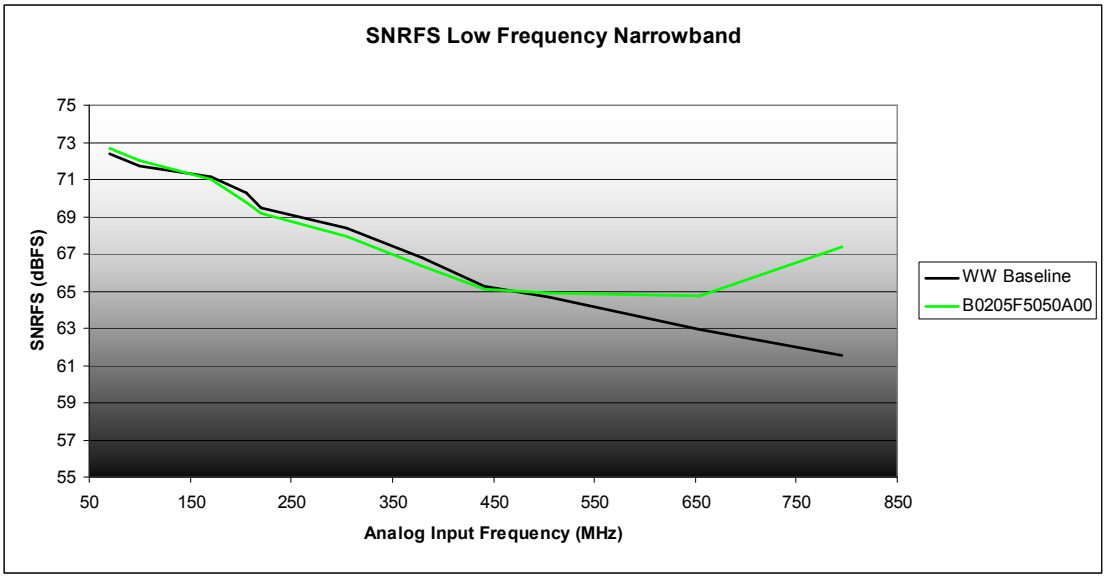


Figure 13 SNR measurement comparison between wirewound baseline and the BD0205F5050A00 with the low frequency tuned network

Wideband Optimized

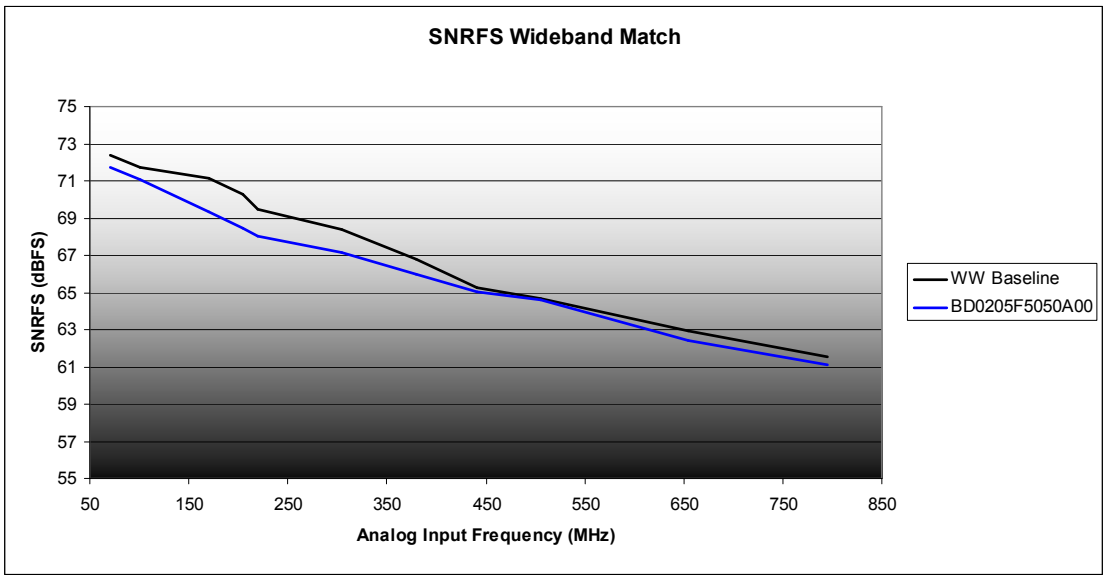


Figure 14 SNR measurement comparison between wirewound baseline and the BD0205F5050A00 for the wideband match case.

Test Setup & Testing Methodology

The results obtained in this application note were obtained using the testing techniques described in *AN-835 - Understanding High Speed ADC Testing and Evaluation* [3].

Roadmap of Future Developments

This applications note has described the use of a multilayer, Merrill structure as a replacement for traditional wirewound transformers. Anaren is also investigating and developing other balun designs to address other outstanding issues in ADC front end design.

Specifically, Anaren design effort is focusing in the following areas:

- 1:4 voltage transformation ratio baluns to reduce input drive requirements
- Lower Frequency 1:1's and 1:4's baluns and possibly 1:2 ratio baluns
- Smaller components for higher frequencies

Summary of Multilayer Advantages

Use of Anaren's multi-layer components will offer the following benefits to the ADC front end designer:

- Improved high frequency amplitude and phase balance resulting in better SFDR at higher frequencies
- Improved gain flatness over wider bands thus reducing input drive requirements
- Smaller footprint and height than traditional wirewounds
- Highly repeatable manufacturing process resulting in little part to part variation
- Ferrite free design thus eliminating the intermodulation and other non-linear effects provided by outside or environmental influences

ADC Performance Parameter Definitions

In this section, some of the more common performance parameters pertaining to ADCs are described. These are taken from Brannon and Reeder[3]:

- **2'nd & 3'rd Order Harmonic Distortion**

The ratio of the rms signal amplitude to the rms value of the second or third harmonic component, reported in dBc.

- **Total Harmonic Distortion (THD)**

The ratio of the rms signal amplitude to the rms sum of all harmonics (neglecting noise components). In most cases, only the first five harmonics are included in the measurement because the rest have negligible contribution to the result. The THD can be derived from the FFT of the ADC's output spectrum. For harmonics that are above the Nyquist frequency, the aliased component is used.

- **Spurious Free Dynamic Range (SFDR)**

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as the signal level is lowered) or DBFS (related back to converter full-scale).

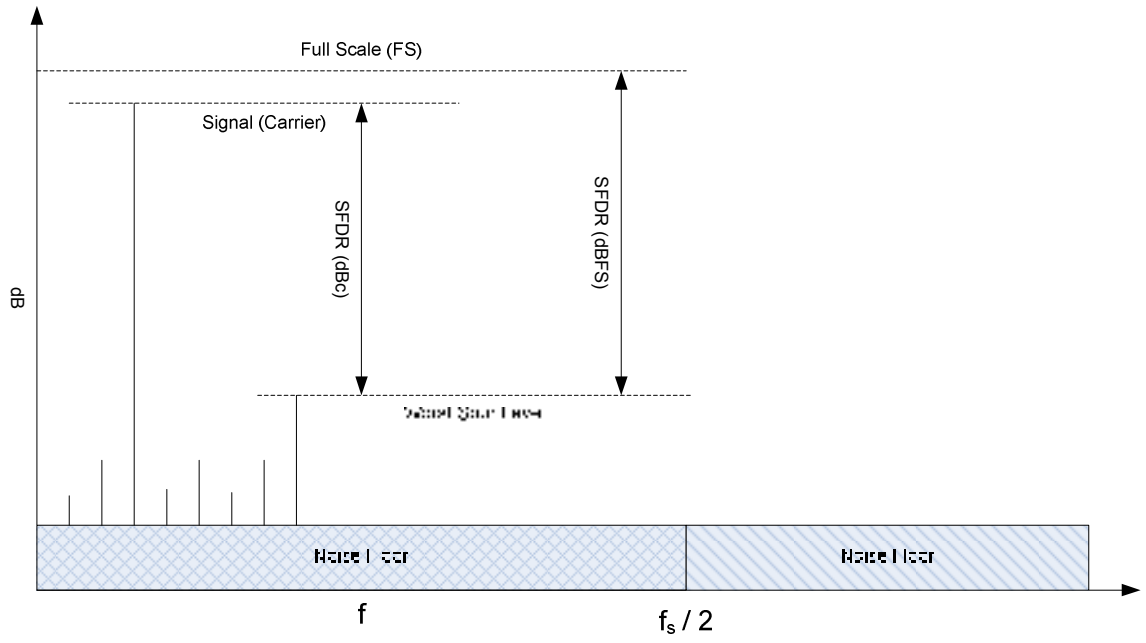


Figure 15 Definition of SFDR

- **Signal-to-Noise-and-Distortion Ratio (SINAD)**

The ratio of the rms signal amplitude (set 1 dB below full-scale to prevent overdrive) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

- **Signal to Noise Ratio (SNR)**

The ratio of the RMS input signal to the RMS value of the sum of all other spectral components below the Nyquist frequency, excluding the first 6 harmonics and DC.

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[2] Analog Devices Datasheet, 14-bit, 105/125 MSPS, IF Sampling ADC AD9445, Rev 0, Analog Devices Ltd., 2005.

[3] Brannon, B, Reeder, R, Analog Devices Application Note, "AN-835 - Understanding High Speed ADC Testing and Evaluation", Analog Devices Ltd., www.analog.com

[4] Analog Devices Application Note, "AN-905 VisualAnalog Converter Evaluation Tool Version 1.0 User Manual", Analog Devices Ltd., www.analog.com

[5] Merrill, J., "Design of Baluns Using Backward Wave Couplers", Applied Microwave & Wireless, vol. 12, #4, April 2000.

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[7] Pokuls R., Woods J;,"Using Anaren's BD0205F5050AHF, BD0310E505AHF Baluns with Analog Devices, Inc AD9445 and AD9446 High Speed Data Converters", Anaren Microwave Ltd., Application Note ANN-9001, July 2009.

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